AMENDMENTS TO THE CLAIMS

Please amend claim 1 and cancel claims 2 and 5 without prejudice, such that the status of the claims is as follows:

1. (Amended) A motor controller for an electric motor having a plurality of motor terminals, the motor controller being connected to a power supply and comprising:

a commutation control connected to the motor terminals for causing current pulses to flow through selected terminals during each commutation state;

a current sensor for providing a sense signal representative of the current pulses;

a peak current target circuit for providing a target signal;

a pulse width control for controlling pulse width of the current pulses as a function of the sense signal and the target signal, wherein the pulse width control includes a comparator which compares the sense signal and the target signal and a pulse generator which supplies a control pulse to the commutation control when the comparator provides an output indicating that the sense signal has reached the target signal; and

a reverse current control for preventing reverse current from flowing into the power supply during change of commutation state, wherein the reverse current control resets the pulse generator at the start of each change of commutation state in which a new motor terminal is connected to a high power supply voltage.

2. (Canceled)

3. (Original) The motor controller of claim 2, wherein the commutation control terminates the current pulse in response to the control pulse from the pulse generator.

4. (Original) The motor controller of claim 1, wherein the peak current target circuit provides the target signal as a function of a current command representative of a desired motor current.

5. (Canceled)

6. (Original) The motor controller of claim 1, wherein the motor has N motor terminals and the commutation control defines 2N commutation states.

7. (Original) The motor controller of claim 6, wherein N = 3.

8. (Original) The motor controller of claim 1, wherein the motor controller is fabricated in an integrated circuit.

9. (Original) A motor controller for controlling speed of an electric motor having a plurality of terminals, the motor controller being connected to a power supply and comprising:

a plurality of motor drivers connected to the plurality of terminals;

sequencer logic for providing control signals to the motor drivers to cause current pulses to flow through selected terminals during each commutation state, the sequencer logic providing a reset signal for preventing reverse current from flowing into the power supply during change of commutation state;

a current sensor for providing a sense signal representative of the current pulses;

a peak current target circuit for providing a target signal which is a function of a current command signal; and

a pulse width control for controlling pulse width of the current pulses as a function of the sense signal, the target signal and the reset signal.

10. (Original) The motor controller of claim 9, wherein the pulse width control includes a comparator which compares the sense signal and the target signal and a pulse generator which supplies a control pulse to the sequencer logic as a function of an output from the comparator and the reset signal.

11. (Original) The motor controller of claim 10, wherein the sequencer logic terminates the current pulse in response to a control pulse form the pulse generator.

12. (Original) The motor controller of claim 9, wherein the current command signal is representative of a desired motor current.

13. (Original) The motor controller of claim 10, wherein the reset signal resets the pulse generator at the start of each change of commutation state in which a new motor terminal is connected to a high power supply voltage.

14. (Original) The motor controller of claim 9, wherein each motor driver includes a first switch connected to the power supply.

15. (Original) The motor controller of claim 14, wherein the reset signal turns off the first switch of a low terminal motor driver at the start of each change of commutation state in which a new motor terminal is connected to a high power supply voltage.

16. (Original) The motor controller of claim 14, wherein the first switch is a MOSFET.

17. (Original) The motor controller of claim 9, wherein the motor controller is fabricated in an integrated circuit.

18-20. (Canceled)

21. (Previously Presented) A motor controller for an electric motor having a plurality of motor terminals, the motor controller comprising:

a plurality of motor drivers connected to the plurality of motor terminals;

sequencer logic for commutating the motor by providing control signals to the motor drivers to drive a first of the motor terminals to a high voltage, drive a second of the motor terminals to an intermediate voltage, and alternately drive a third of the motor terminals between the high voltage and a low voltage; and

reverse current control for driving the third motor terminal to the low voltage upon the occurrence of a high side commutation.

22. (Previously Presented) The motor controller of claim 21 and further comprising:

a pulse width modulator for generating a pulse width modulated signal for use by the sequencer logic in alternately driving the third of the motor terminals between the high voltage and the low voltage.

23. (Previously Presented) The motor controller of claim 22 wherein reverse current control is logic residing in the sequencer logic for detecting the occurrence of a high side commutation and for providing a reset signal to the pulse width modulator upon the occurrence of a high side commutation.

24. (Previously Presented) The motor controller of claim 23, wherein the pulse width modulator comprises:

a current sensor for providing a sense signal representative of the current flowing through the motor;

a peak current target circuit for providing a target signal which is a function of a current command signal; and

a comparator which compares the sense signal and the target signal; and

a pulse generator which supplies a control pulse to the sequencer logic as a function of an output from the comparator and the reset signal.